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Performance Improvement of 4-Bit Static CMOS Carry Look-Ahead Adder Using Modified Circuits for Carry Propagate and Generate Terms

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Abstract: Carry Look-Ahead Adder (CLA) is considered as one of the most widely used adder topologies which are used in high performance computing systems. In this research, an improved version of 4-bit CLA adder has been proposed. Performance improvement of 4-bit CLA adder has been made by using hybrid AND and XOR gates in the input side for generating carry propagate and carry generate terms. The CLA circuits are kept exactly the same as the conventional one. Performance of the proposed modified 4-bit CLA adder has been evaluated and compared with the conventional design using Cadence tools in 90 nm technology node. Performance has been evaluated and compared in terms of average power, propagation delay and power delay product. The proposed modified design exhibited significant improvement in performance while compared with the conventional one. Enhancement done by the proposed 4-bit CLA adder design in average power, propagation delay and PDP were 14.96%, 11.76% and 25.32% respectively. In addition to performance enhancement, transistor count require for the proposed design is quite less compared to the conventional design which result in less surface area on chip. Moreover, less transistor count accounts for less power dissipation. Hence, utilizing the proposed design in modern high-performance computing systems would bring about high-performance improvements.

Keywords: Carry Look-ahead Adder, 4-Bit Adder, Xor Gate, And Gate, Carry-Propagate

1. Introduction

The revolution in semiconductor industry have resulted in producing modern compact, smart and intelligent electronic devices where performance of microelectronic circuits plays crucial role [1-10]. Hence, optimization of performance parameters of integrated circuits is a must.

Arithmetic Logic Unit (ALU) of modern integrated circuits are responsible for binary arithmetic operations which need to be efficient [11]. Adding binary numbers in one of the key operations of ALU [12]. Moreover, binary multiplication, subtraction and division requires addition of binary bits [13-15]. Hence, performance optimization of adder circuit would bring about overall impact on the performance of ALU [16]. Therefore, researchers and academicians are continuously working on developing and implementing new adder designs for better performance [17].

Full Adder cell is the basic cell for addition of two binary bits [18-19]. However, in modern processors, implementation of wide adders is required. Ripple Carry Adder (RCA) based on 1-full adder is the basic technique for implementation of wide adders [20-21]. However, propagation delay obtained using RCA in long carry chains in quite high for which it became quite impractical to use RCA in high performance devices [22-23]. In order to solve the carry propagation delay in long carry chains, several Parallel-Prefix Adder topologies have been developed [24]. CLA adder is one of the PPA topologies which reduces carry propagation delay by using a complex circuitry using carry-propagate and carry-generate terms [25]. Although, CLA adder enhances performance in

speed by reducing propagation delay, transistor count is quite high in CLA adder compared to RCA. This high transistor count results in high area consumption in chip. In addition, it results in high power dissipation [26].

Static CMOS logic based CLA adders are most common and widely used adder topology due to its high robustness and driving power. However, using complementary pair of N-channel CMOS (NMOS) and P-channel CMOS (PMOS) makes the number of transistors in circuit high. This high number of transistors accounts for high input impedance for signals. As a result, delay increases due to increased RC time constant. However, an improvement can be achieved by utilizing a combination of static CMOS logic with other logic techniques. This sort of combination of several logic techniques is called hybrid logic style [27-29]. Nowadays, hybrid logic styles using different logic techniques are attracting the attention among researchers and circuit designers.

This research aims to enhance the performance of conventional static CMSO logic based 4-bit CLA adder by employing hybrid logic style. The propose design uses a combination of Static CMOS logic, Pass Transistor Logic (PTL) and Transmission Gate (TG) Logic. In order to validate the performance of the proposed CLA circuit, verification has been done by conduction simulation using Cadence design tools [30]. Technology node for performance evaluation has been set to 90 nm. Both the proposed and the conventional designs of 4-bit CLA adder circuits were simulated and results have been compared to have the overall idea of improvement made by the proposed design. However, different hybrid designs have their different pros and cons for which they are often application specific. Hence, it is required to take proper care while using hybrid logic based on the application and the operations conditions of the circuit.

The remaining portion of this research article has been organized as follows. In section II, literature review and circuit design technique for conventional design have been stated. Detailed information of proposed hybrid CLA adder has been stated in section II. The following section discloses the simulation results obtained using Cadence tools. Performance comparison between existing and proposed designs have been done in section IV. In the end, concluding comments based on the observations as per simulation results have been stated.

2. Conventional 4-Bit CLA Adder Design Methodology

In Ripple Carry Adder (RCA), input carry term of one block comes form the output carry term of the previous blocks. Therefore, one block needs to wait for its previous block to finish its computation in order to get its input carry signal. This carry generation process in RCA causes the entire adder circuit to response very slowly which is not accepted in modern high-speed computational systems. Hence several PPAs have been developed over the course of time in order to enhance computational speed. CLA adder takes the input terms and drive them in a CLA process in order to create the carry-terms all at a time so that the carry input signal of one block does not have to wait for the carry-out signal of the previous block.

As per discussed in [31], block diagram of conventional design of 4-bit CLA adder is represented by Figure 1. A 4-bit CLA adder has two major parts: carry generation part and sum generation part. If A and B are considered as the input bits, then the Formula for carry and sum generation can be written as follows [32].

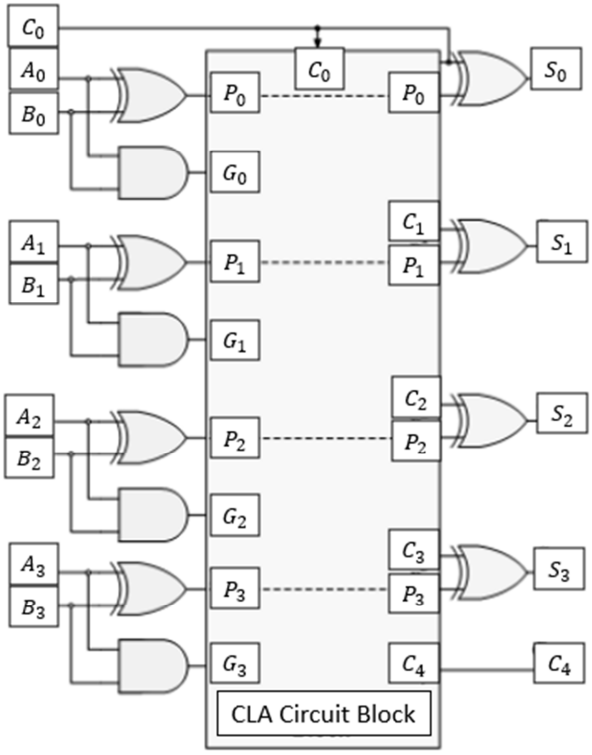

Figure 1. *Block diagram of 4-bit CLA adder.*

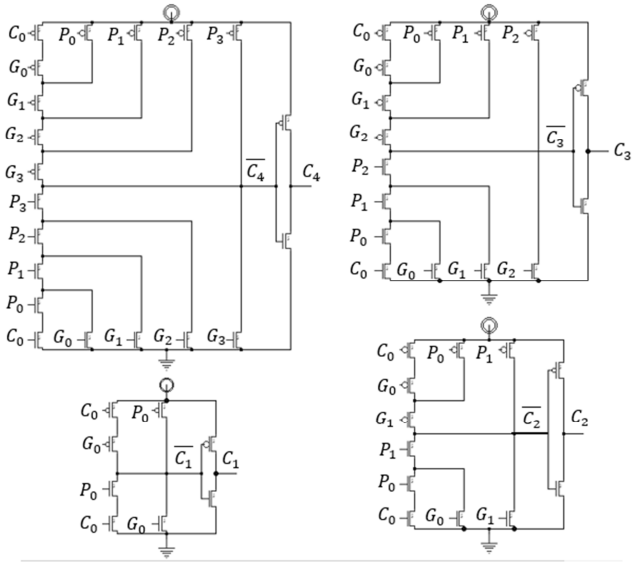

Figure 2. *Circuit design of CLA terms in conventional static CMOS logic.*

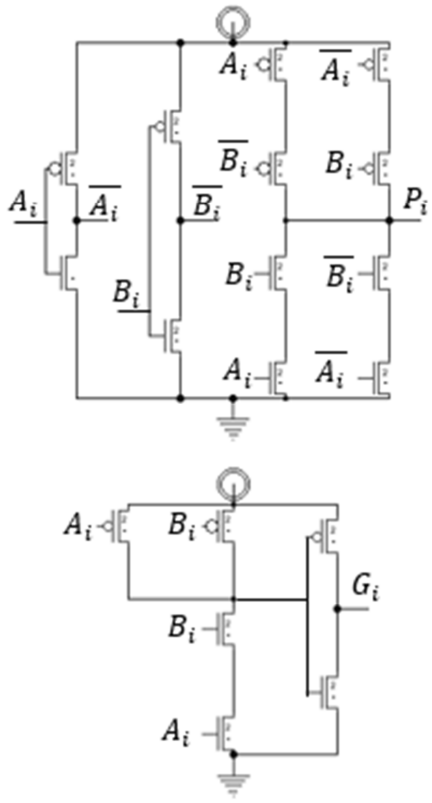

Figure 3. *XOR and AND gate Design used in conventional CLA adder.*

$$C_{i+1}=G_i+P_iC_i$$

$$S_i=P_i \oplus C_i$$

where,

$0< i < 3$ and "i" is integer number

C=Carry terms

$G_i=AB$ (Carry Generate Term)

$P_i=A_i \oplus B_i$ (Carry Propagate Term)

Based on the observations on the equations stated above, it can be clearly said that the carry generation circuit would require AND and XOR gate since the Boolean expression of the G_i and the P_i terms represents AND and XOR operations respectively. As per [33], CLA circuits for 4-bit CLA adder are represented in Figure 2. The circuits for designing G_i and P_i terms are depicted by Figure 3.

In conventional design, the AND gate and XOR gate depicted in Figure 3 are used for generating the gate input signals in Figure 3. After generating the G_i and the P_i terms by using the AND and XOR gates, the CLA circuits depicted in Figure 2 generates the carry-out terms. Since all carry terms are generated all at a time using the CLA circuits, carry term of one block does not need to wait for its previous block to compute carry-out signal. In this way, CLA process reduces the carry propagation delay in adder circuit.

3. Proposed Hybrid Circuit Design of 4-Bit CLA Adder

In order to enhance performance of the conventional design of 4-bit CLA adder, transistor count needs to be reduced in order to achieve low input impedance. In order to reduce input impedance, the input circuits where the signals are fed needs to be re-designed in order to reduce transistor count. Moreover, reducing the transistor count would result in reducing the size of the entire adder circuit for which area requirement of the adder in chip would be decreased. In addition, decreasing the transistor count will make the circuit power efficient because power consumption of the circuit would decrease. Since the input circuits are the G_i and P_i circuits which are nothing but AND and XOR gates, therefore using new efficient AND and XOR gates would result in better performance. The CLA circuits for C_4, C_3, C_2 C_1 and sum generation circuits for S_4, S_3, S_2 S_1 in the output side are kept in as per static CMOS logic style. Since static CMOS logic provide better driving capability, it would be highly beneficial for the design if static CMOS logic is kept at the outermost terminal.

The idea of the modification done in this research work is to utilize static CMOS circuit in the output side terminals so that the circuit becomes robust and have high driving power. At the same time, efficient AND and XOR gates employing hybrid logic style and having low transistor count are placed in the input side terminals so that the transistor count as well as the input impedance become reduced. Moreover, the power dissipation and adder area would be also reduced due to employing AND and XOR gates that has low transistor count. In this way, the proposed circuit has driving power and robustness of static CMSO logic. At the same time, performance has been also improved by using efficient hybrid gates in the input side terminals for generation of G_i and P_i terms. The AND gate and XOR gates used in this research are adopted form [27] since the performance of the AND and XOR gates in [27] are high compared to the others. The AND and XOR gates used in this research work for G_i and P_i circuits are presented using Figure 4 and Figure 5 respectively.

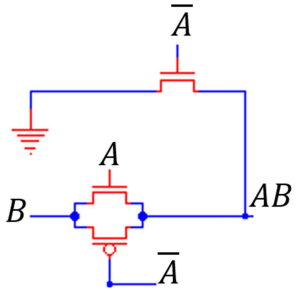

Figure 4. *AND gate design used in proposed 4-bit CLA adder to generate Gi terms [27].*

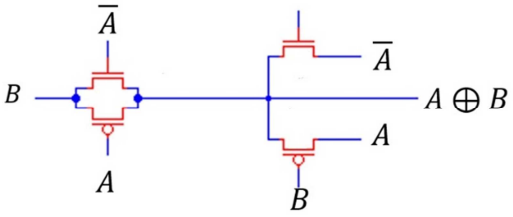

Figure 5. *XOR gate design used in proposed 4-bit CLA adder to generate Pi terms [27].*

Table 1. *Table information.*

CLA Adder	Performance Parameter	Simulation result	Improvement
Existing	Power (µW)	27.4	14.96%
Proposed		23.3	
Existing	Delay (ns)	0.17	11.76%
Proposed		0.15	
Existing	PDP (fJ)	4.66	25.32%
Proposed		3.48	

4. Simulation Result

In order to prove the performance improvement of the proposed design of 4-bit CLA adder, simulation has been conducted of proposed and existing designs. Performance of the circuits were evaluated in terms of average power, propagation delay and Power Delay Product (PDP). PDP is the product of propagation delay and Average Power of a circuit. For simulation purpose, the supply voltage for all the simulation runs were fixed to 1.2 V in order to simulate the circuits under a common environment.

Obtained results using Cadence Design Tools are presented in Table 1. In addition, the results have been reported graphically using Figures 6-8.

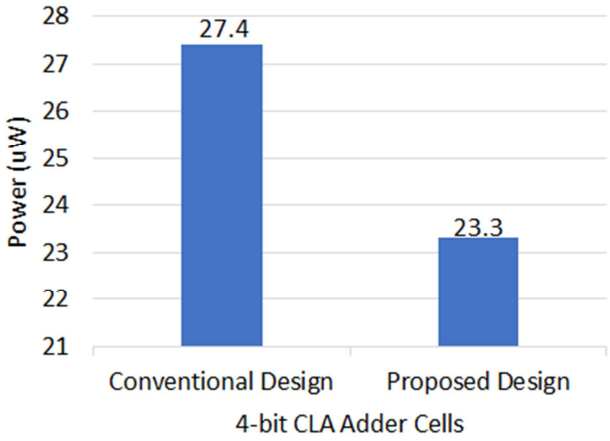

Figure 6. *Average power comparison.*

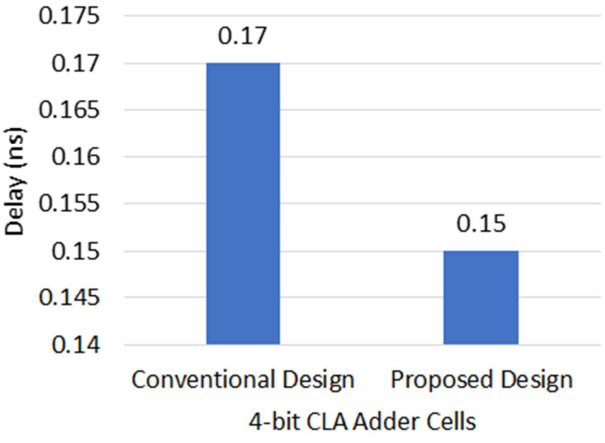

Figure 7. *Propagation delay comparison.*

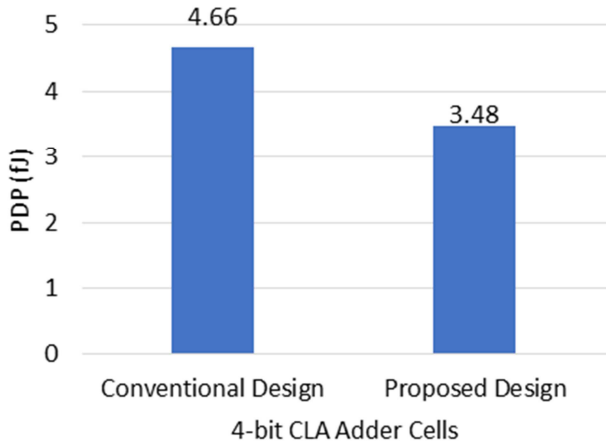

Figure 8. *PDP comparison.*

5. Discussion and Comparative Analysis

After observations of Table 1 and Figures 6-8, it can be seen the proposed design of 4-bit CLA adder has obtained superior performance than the existing one in all the performance aspects considered.

In addition to the performance enhancement, transistor count of the proposed CLA 4-bit adder is lower than the existing one. This resulted in less area which is an important factor while designing CMOS circuit [34-36].

Although the proposed design used hybrid AND and XOR gate rather than using robust and high driving power acquainted static CMOS logic baste AND and XOR gates, the overall advantage of static CMOS style in the proposed design remains same as the existing one. It's because driving capability is required in the output terminal so that the circuit can perform well in high fan-out conditions. Since, the proposed design contains static CMOS logic in the output terminals, advantages of the conventional design remain unchanged in the proposed design.

6. Conclusion

A modified hybrid 4-bit CLA adder has been proposed in this research work. The modified design displayed significant enhancement in performance. The performance enhancements in average power, propagation delay and PDP were 14.96%, 11.76% and 25.32% respectively. Moreover, due to the less transistor count of the design, the area on chip has been reduced. Low transistor count also accounted for less power dissipation while compared with conventional 4-bit CLA adder topology. Therefore, according to the simulation results, it is verified that the proposed 4-bit CLA adder offers better performance for which it becomes quite worthy to be used in modern devices.

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